REMARKS

Claims 1-3, 6-11, 14-16, 20, 22-24, 26-33 and 52-54 are pending in the application.

Claims 1-3, 6, 7, 10, 11, 14-16, 20, 24, 26-29, 32, 33 and 52-54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art of Figures 1A-1B in view of Yoshinori (JP 63-9968).

Claim 1 recites an image sensor comprising "a substrate formed over a base layer; a plurality of pixel cells formed within said substrate, each pixel cell comprising a photo-conversion device having a charge collection region of a second conductivity type for accumulating photo-generated charge formed in said substrate below a first layer of a first conductivity type; and a plurality of trenches, each trench being provided along a perimeter of a respective pixel cell, each trench extending at least to a surface of the base layer and below a lower level of said photo-conversion device, each trench having sidewalls, and being at least partially filled with a material that inhibits electrons from passing through said trench, wherein each of said plurality of trenches prevents diffusion of photo-generated charge generated by said photo-conversion device in one pixel cell to an adjacent pixel cell." The combination of AAPA with Yoshinori does not achieve a structure having the limitations of claim 1. Reconsideration is therefore respectfully requested.

The claimed invention relates to a deep trench isolation structure and method for reducing crosstalk among semiconductor circuits and particularly, among adjacent photoconversion devices formed in pixel circuits. In one embodiment, a trench is etched into a substrate adjacent to a photoconversion device region, wherein the trench extends to an epitaxial layer below the substrate. (Present Application, ¶ [0011]) The deep trench

inhibits electrons from diffusing under the isolation trench to an adjacent pixel. (Present Application, ¶ [0031]) Yoshinori and the AAPA, even if considered in combination, still fail to teach or suggest the claimed invention.

The Examiner contends that Yoshinori discloses all of the limitations of claim 1. Particularly, the Examiner cites to reference characters 2 and 1 in Figure 6 of Yoshinori as the substrate and the base layer, respectively, and contends that Yoshinori discloses the limitation "[a] trench extending at least to a surface of [a] base layer and below a lower level of [a] photoconversion device." (Office Action, pp. 3, 9) Applicant respectfully disagrees. A machine translation of Yoshinori (obtained by the Applicant and a copy of which is enclosed herewith) reveals that Figure 6 of Yoshinori shows that the pinphotodiode consists of diffusion layer 4, epitaxial layer 2 and substrate 1. (second full paragraph of Yoshinori translation, page 3). The reference characters 2 and 1 are epitaxial layer and substrate, respectively and not what the Examiner contends these reference characters to be. Further, the Yoshinori trench stops at the substrate 1. Thus, the trench 3 in Yoshinori Figure 6 is not below a lower level of the Yoshinori pinphotodiode. Particularly, Yoshinori does not disclose or teach "each trench extending at least to a surface of the base layer and below a lower level of said photo-conversion device."

In addition, there is no motivation or reason to combine the AAPA with Yoshinori. Yoshinori is directed to increasing the threshold of a parasitic MOS transistor using an element separation method. (Yoshinori translation, page 1) The AAPA, on the other hand, relates to a photo-conversion device having pixel cells which are isolated from one another by shallow trench isolation (STI) regions. There is no reason to combine AAPA's photo-conversion device with Yoshinori's parasitic MOS transistor to achieve the claimed invention. It appears that the proposed combination of AAPA and Yoshinori is

merely an attempt to reconstruct the claimed invention using Applicant's own disclosure as a roadmap. Therefore, Applicant respectfully requests that the rejection of independent claim 1 and its dependent claims 2-3, 6, 7, 10, 11 and 52-54 be withdrawn and the claims allowed. Claims 14-16, 20, 24, 26-29, 32 and 33 contain similar limitations as claim 1 and therefore, the rejection of these claims should also be withdrawn.

Claim 14 recites a structure for isolating an active area on a semiconductor device comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, wherein said trench extends at least to a surface of a base layer below said substrate which is below a lower level of said photo-conversion device, and wherein said trench has sidewalls." For the above-mentioned reasons, claim 14 and its dependent claims 15-16, 20 and 24 are likewise allowable.

Claim 26 recites a processor system comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, the active area having a photo-conversion device comprising a charge collection region of n-type conductivity for accumulating charge and located below a p-type region of said active area, wherein said trench extends at least to a surface of a base layer below said substrate and to a level below a lower level of said photo-conversion device, and wherein said trench has sidewalls and inhibits diffusion of charge outside said active area." For the above-mentioned reasons, claim 26 and its dependent claims 27-29, 32 and 33 are likewise allowable.

Claims 8, 9, 22, 23, 30 and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art of Figures 1A-1B in view of Yoshinori in view of Clevenger. (US 2004/0227061).

Claims 8 and 9 depend from claim 1 and as such, recite an image sensor, comprising, in part, "a photo-conversion device having a charge collection region of a second conductivity type for accumulating photo-generated charge formed in said substrate below a first layer of a first conductivity type; and a plurality of trenches, each trench being provided along a perimeter of a respective pixel cell, each trench extending at least to a surface of the base layer and below a lower level of said photo-conversion device, each trench having sidewalls, and being at least partially filled with a material that inhibits electrons from passing through said trench, wherein each of said plurality of trenches prevents diffusion of photo-generated charge generated by said photo-conversion device in one pixel cell to an adjacent pixel cell."

Claims 22 and 23 depend from claim 14 and as such, recite a structure for isolating an active area on a semiconductor device comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, wherein said trench extends at least to a surface of a base layer below said substrate which is below a lower level of said photo-conversion device, and wherein said trench has sidewalls."

Claims 30 and 31 depend from claim 26 and as such, recite a processor system comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, the active area having a photo-conversion device comprising a charge collection region of n-type conductivity for accumulating

charge and located below a p-type region of said active area, wherein said trench extends at least to a surface of a base layer below said substrate and to a level below a lower level of said photo-conversion device, and wherein said trench has sidewalls and inhibits diffusion of charge outside said active area."

As mentioned earlier, the AAPA when in combination with oshinori fails to disclose, teach or suggest all of the limitations of claims 1, 14 and 26. Clevenger fails to cure the deficiencies of Yoshinori and the AAPA. The Office Action relies on Clevenger to only teach a trench depth greater than about 2000 Angstroms and an image sensor. (Office Action, p. 8) Therefore, Applicant respectfully requests that the rejection of claims 8, 9, 22, 23, 30 and 31 be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

Dated: April 8, 2008

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Ranga Sourirajan
Registration No.: 60,109
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant

ELEMENT ISOLATION OF ELECTROSTATIC INDUCTION TRANSISTOR IMAGE SENSOR

Bibliographic Fields

Publication number:	JP63009968
Publication date:	1988-01-16
Inventor:	OOTA YOSHINORI
Applicant:	OLYMPUS OPTICAL CO
Classification:	
- international:	***H01L21/76; H01L27/146; H04N5/335;*** **H01L21/70; H01L27/146; H04N5/335;** (IPC1-7): H01L21/76; H01L27/14; H04N5/335
- European:	H01L27/146S
Application number:	JP19860152707 19860701
Priority number(s):	JP19860152707 19860701

Abstract

PURPOSE:To invert an Si surface in the bottom of a trench even under any bias conditions, and to form a parasitic channel by increasing the first impurity concentration of a first semiconductor substrate being in contact with the cut trench in the first semiconductor substrate containing a first impurity and isolating an element. CONSTITUTION:A trench is dug to an Si substrate on which an epitaxial layer 2 is shaped, and an N-type impurity is doped to Si on the inside of the trench by using Pocl3, phosphorus-doped SiO2, arsenic-doped SiO2, etc., as an Si surface except the trench is left as it is masked. Si in the trench is insulated by a thin thermal oxide film 26, and the trench is buried with non-doped polysilicon 27. Polysilicon 27 in the trench and the surface of the Si substrate are oxidized to form a thick oxide film 28, and subsequent processes are executed, thus shaping a p<+> gate 29. Accordingly, the threshold of a parasitic MOS transistor can be increased, and channels between gates in adjacent elements can be turned OFF at all times even under any bias conditions during the operation of an image sensor.

明細書

Specification

1.発明の名称

静電誘導トランジスタイメージセンサの素子分離法

1.Title of Invention

element separation method of electrostatic induction transistor image sensor

Claims

2.特許請求の範囲

(1)

静電誘導トランジスタを光電変換素子として構成されるイメージセンサの第 1 不純物を含む第 1 半導体基板に溝を掘り、該溝の内面に絶縁膜を被着しポリシリコンで溝を埋め戻して素子を分離する方法において、前記溝に接する第 1 半導体基板の第 1 不純物濃度を高めることを特徴とする静電誘導トランジスタイメージセンサの素子分離法。

2.Claim (s)

(1)

Digging slot in first semiconductor substrate which includes first impurity of image sensor which configuration is done with electrostatic induction transistor as photoelectric conversion element ,applying insulating film to interior surface of said slot and burying slot with polysilicon and resetting and regarding to method whichseparates element , element separation method . of electrostatic induction transistor image sensor whichdesignates that it raises first impurity concentration of first semiconductor substrate which touches to theaforementioned slot as feature

(2)

前記溝の底部に接する第 1 半導体基板の第 1 不純物濃度を選択的に高めることを特徴とする特許請求の範囲第 1 項記載の静電誘導トランジスタイメージセンサの素子分離法。

(3)

静電誘導トランジスタを光電変換素子として構成されるイメージセンサにおいて、第 1 不純物を含む第 1 半導体基板に溝を掘り、該溝の側面にのみ絶縁膜を被着し、ポリシリコンで溝を埋め戻すことを特徴とする静電誘導トランジスタイメージセンサの素子分離法.

(4)

前記ポリシリコンは、ノンドープポリシリコンであることを特徴とする特許請求の範囲第 3 項記載の静電誘導トランジスタイメージセンサの素子分離法.

(5)

前記ポリシリコンは、第 1 不純物を含むポリシリコンであることを特徴とする特許請求の範囲第 3 項記載の静電誘導トランジスタイメージセンサの素子分離法。

(6)

前記溝の側面にのみ絶縁膜を被着し、該溝の底部の第 1 半導体基板の第 1 不純物濃度を高めた後、ノンドープポリシリコンで埋め戻すことを特徴とする特許請求の範囲第 3 項記載の静電誘導トランジスタイメージセンサの素子分離法。

Specification

3.発明の詳細な説明

(産業上の利用分野)

この発明は、静電誘導トランジスタ(SIT)を光電変換素子として構成されるイメージセンサの素子分離法に関する.

〔従来の技術〕

近年、撮像デバイスの固体化は急速に進みつつあり、例えばCCD 型,MOS 型固体撮像素子を用いたビデオカメラが市場に出回っている。固

(2)

element separation method . of electrostatic induction transistor image sensor which is stated in Claim 1 which designates thing which first impurity concentration of first semiconductor substrate which touchesto base of aforementioned slot selectively is raised asfeature

(3)

element separation method . of electrostatic induction transistor image sensor which designates that you dig slot in first semiconductor substrate which includes first impurity , in image sensor which configuration is done with electrostatic induction transistor as photoelectric conversion element , apply insulating film to only side face of said slot , bury slot with the polysilicon and reset as feature

(4)

As for aforementioned polysilicon , element separation method . of electrostatic induction transistor image sensor which is stated in Claims Claim 3 which designates that it is a non doped polysilicon as feature

(5)

As for aforementioned polysilicon , element separation method . of electrostatic induction transistor image sensor which is stated in Claims Claim 3 which designates that it is a polysilicon which includes first impurity as feature

(6)

It applies insulating film to only side face of aforementioned slot ,after raising first impurity concentration of first semiconductor substrate of base of said slot , itburies with non doped polysilicon and element separation method . of electrostatic induction transistor image sensor whichis stated in Claims Claim 3 which designates that you reset as feature

3.Detailed Description of the Invention

(Industrial Area of Application)

this invention regards element separation method of image sensor which configuration is donewith electrostatic induction transistor (SIT) as photoelectric conversion element .

[Prior Art]

Recently, solidification of camera device is advancing quickly, for example CCD array type, the video camera which uses MOS type solid state camera element has arrive

体撮像素子の応用分野はホームビデオカメラに限らず、視覚センサとして工業用ロボット,防犯カメラ、天文観測、スチルカメラ等の多方面に広がっている。かかる固体撮像素子に対する要求項目の一つに高感度化がある。スチルカメラの実用化,映像の高品質化,ビデオカメラの超小型化に対する強いニーズに応えるためには、撮像素子の高感度化が必須の要件になっている。

d to market . applied field of solid state camera element is spreading to industrial robot , crime prevention camer a , astronomical observationand still camera or other pol yhedron not just home video camera , as visual sensor . There is a increasing sensitivity in one of requirement f or this solid state camera element . In order to answer t o strong needs where it confronts ultraminiaturization of quality increase , video camera of utilization and image of still camera , increasing sensitivity of the photographi c element has become necessary requisite .

SITを光電変換素子として用いるラインセンサや固体撮像素子は、光電荷を素子内部で増幅できるため、高感度イメージセンサとしての期待が持たれている。第6図はSITイメージセンサが高感度であることに着目して、1つのセル寸法を縮小し、微細なセルで構成したSITイメージセンサのセルの断面を示す図であり、n'基板1をドレインとし、その上に成長させたn-エピタキシャル層2内にトレンチ分離部3で分離されたSITセルI, II,III がアレイ状に配置されている状態を示している.1つのセルはp'拡散層4で形成されるゲート、浅いいn'拡散層5で形成されるソース、及びゲート容量を形成するための薄いゲート酸化膜6及び該酸化膜6上に形成されたポリシリコン7、並びにソースを形成するn'拡散層5からコンタクトを取るためのポリシリコン8からなっている。そしてゲート酸化膜6,ソース拡散層5以外のシリコン表面は厚い酸化膜9で覆われている。

As for line sensor and solid state camera element which use SIT as photoelectric conversion element , the photo charging amplifying because it is possible with element i nterior , expectation as high sensitivity image sensor lean s. Figure 6 paying attention to SITimage sensor being hi gh sensitivity , reduces the cell dimension of one , in fi gure which shows cross section of cell of SITimage sens or which configuration is done, designates n'substrate 1 a s the drain with microscopic cell , In order to form sour ce , and gate capacity which as for cell ofthe.one which has shown state where SITcell I, II, III which is separa tedinside n- epitaxial layer 2 which grew on that in tren ch isolation section 3 is arranged in array gate , which i s formed with p'diffusion layer 4 it is shallow areand ar e formed with n'diffusion layer 5 thin gate oxide film 6 and It has consisted of polysilicon 8 in order to take co ntact from the polysilicon 7, which was formed on said oxide film 6 and n'diffusion layer 5 which forms the sou rce . And as for silicon surface other than gate oxide fil m 6, source diffusion layer 5 it is covered with thick ox ide film 9.

このように構成されているSITセルにおける光電変換は、p'ゲート拡散層4,n-エピタキシャル層2,n'ドレイン基板1からなるpinホトダイオードで行われる.光蓄積期間に、このホトダイオードは逆バイアスされ、光入射によって発生する電子はn'ソース拡散層5かn'ドレイン基板1へ逃げ、ホールはp'浮遊ゲート拡散層4に蓄積され、ゲート電位を上昇する.そして光電荷によるゲート電位の増加分が、光信号読み出し期間中に、ポリシリコン7,ゲート酸化膜6p'ゲート拡散層4からなるゲート容量を介してp'ゲート拡散層4に加えられるゲートバイアス電圧に加算されるため、ソース拡散層5とドレイン基板1との間には光電荷の蓄積量に対応する大きな出力電流が流れ、光信号が読み出される。SITイメージセンサのセル構成は、光電変換と増幅作用とが1つのSIT内で行われるため、1つのセル当たり1個のトランジスタでよく、微細化には適している。SITイメージセンサの微細化を行うには、素子分離領

this way as for photoelectric conversion in SITcell which configuration is done,in the.optical storage time which is done with pinphotodiode which consists of p'gate diffusi on layer 4, n- epitaxial layer 2, n'drain substrate 1,as for this photodiode reverse bias it is done, electron which occurs withoptical incidence escapes to n'source diffusion layer 5 or n'drain substrate 1, hole the compilation is d one in p' floating gate diffusion layer 4, gate voltage ris es. And with photocharging increased fraction of gate vo ltage , in light signal reading time , polysilicon 7, gate oxide film 6p' [ge] - through gate capacity which consi sts of * diffusion layer 4,because it is added to gate bia s voltage which is added to p'gate diffusion layer 4,corre sponds to stored amount of photocharging between sourc e diffusion layer 5 and drain substrate 1 large output cur rent to flow, light signal reads out. cell configuration of SITimage sensor , because photoelectric conversion and a mplifying action are doneinside SIT of one , may be tra nsistor of per cell 1 of the one , suitable for narrowing

域の縮小化が問題であり、この点を解決する手段として、第 5 図に示すようにトレンチ分離法がとられている。トレンチ分離部 3 は分離領域に異方性エッチングにより溝を掘り、溝表面を熱酸化膜等の絶縁膜 10 で絶縁した後、通常ノンドープポリシリコン 11 で埋め戻し平坦化して形成される。この時の分離幅はシリコン異方性エッチングのマスク幅で決まり、1μm 程度の分離幅は容易に達成できる。

is. To do narrowing of SITimage sensor , reduction of d isassociated element region being problem ,as shown in Figure 5 , as means which solves this point,trench isolati on method is taken. trench isolation section 3 you dig sl ot in disassociation region with anisotropic etching , the slot surface with thermal oxide film or other insulating fi lm 10 insulating after doing, you bury usually with the non doped polysilicon 11 and reset and planarization do and are formed. Separation width at time of this is decid ed with the mask width of silicon anisotropic etching , c an achieve separation width of 1;mu m extent easily.

第 6 図の SIT セル I は、n'基板 1 まで到達する深いトレンチ分離部 3 によって SIT セル II,III から絶縁される。トレンチ分離部 3 はボロン拡散に対するストッパとしても働くので、トレンチ分離部 3 を形成してから p'ゲート拡散を行えば、p'ゲート拡散層 4 はトレンチ分離部 3 のところで止まる。すなわちトレンチ分離部 3 と p'ゲート拡散層 4 とを直接接触させることができるので、トレンチ分離法は SIT 微細化セルの分離法として適しているものである.

(SITcell I of Figure 6 to n substrate 1 arrives in deep tre nch isolation section 3 insulating is done from SITcell I I, III. After trench isolation section 3 as stopper for boro n scattering because it works,forming trench isolation sec tion 3, if p'gate scattering is done, p'gate diffusion layer 4 stops at theplace of trench isolation section 3. Namely because direct contact it is possible trench isolation sect ion 3 and p'gate diffusion layer 4,trench isolation method is something which is suitable as separation method of SITnarrowing cell .

(発明が解決しようとする問題点)

トレンチ分離法を SIT セル分離に用いる時に、注意すべき点は、アレイ動作において隣接 p'ゲートに異なる電圧が加わった時に、両 p'ゲート間に寄生チャンネルができる可能性があることである。例えば第 7 図(A)に示すように、トレンチ分離部 15 が浅くトレンチ底部 16 の不純物濃度が低い場合には、隣接ゲート G1,G2 に異なる電圧、例えばゲート G2 に電圧 Vcc が加わっていると、トレンチ側面 17 及び底部 16 の N 型シリコン表面が反転し P 型チャネル 18 を形成し、両ゲート G1,G3 が導通してしまう可能性がある.

(Problem That Invention Seeks to Solve * problem)

When using trench isolation method for SITcell portion s eparation, as for point whichshould note, when different voltage joins to adjacent p'gate at time of array operatin g, it is to be possibility which can designate parasitism channel asbetween both p'gate . Way it shows in for exa mple Figure 7 (A), when trench isolation section 15 to be shallow the impurity concentration of trench base 16 is low, when voltage Vcc has joined to different voltage , for example gate G2 in adjacent gate G1, G2, n-type silicon surface of trench side face 17 and base 16 does i nverting and the p-type channel 18 is formed, both gate G1, G3 is a possibility which continuity is done.

第 7 図(A)の等価回路を第 7 図(B)に示す。SIT のドレイン基板 1 には、アレイ動作中一定の正電圧 Vn が加えられており、分離部 15 内のポリシリコン 19 にはゲート G2 の電圧 Vcc が寄生容量 C1 と C2 とに分割されて加わるので、トレンチ内ポリシリコン 19 の電圧 Vpos は次式で与えられる。トレンチ内ポリシリコン 19 は通常ノンドープなので非常に大きな抵抗 20 を持っており、ポリシリコン 19 の電圧はゲート電圧 Vcc の変化に瞬時に追随して上式の値になることはないが、隣接ゲート G1,G2 間に寄生容量 C1,C2 と寄生抵抗 20 でバイアスされる浮遊寄生 MOS トランジスタ 21 が存在することになり、これは正常なアレイ動作を阻害することになりかねない。

equivalent circuit of Figure 7 (A) is shown in Figure 7 (B). During array operating fixed positive voltage Vn t o be added by drain substrate 1 of the SIT, voltage Vcc of gate G2 being divided with by parasitic capacitance C1 and the C2 into polysilicon 19 inside separation porti on 15, because it joins, voltage Vpos of polysilicon 19 i nside trench is given with next formula . Because polysil icon 19 inside trench usually is non doped , we have th e resistor 20 which is large to unusual , as for voltage of polysilicon 19 following to moment in change of gate voltage Vcc, there are not timeswhen it reaches value o f above equation . Between adjacent gate G1, G2 with p arasitic capacitance C1, C2 and parasitic resistance 20 it is decided that thefloating parasitism MOS transistor 21 which bias is done exists, this is not unable tocome to p

oint of inhibition doing normal array operation.

上記第 6 図と第 7 図(A)には、それぞれ極端な例として、トレンチ分離部の底部がn'基板 1 まで達している場合と、トレンチ分離部の底部がエピタキシャル層 2 内にあり該トレンチ底部 16 の不純物濃度が十分低い場合を示した。実際の SIT イメージセンサのエピタキシャル層の不純物濃度の深さ方向のプロファイルbは、第8図に示すようにプロセス中の熱処理の影響を受けて、n'基板からSbがエピタキシャル層表面に向かって拡散するため、エピタキシャル層形成時の不純物濃度プロファイル a とは大きく異なり、徐々に変化している。

In above-mentioned Figure 6 and Figure 7 (A), base of trench isolation section has reached to n'substrate 1 as r espective extreme example,when and, base of trench isola tion section was inside epitaxial layer 2 and the impurity concentration of said trench base 16 showed case where fully it is low. profile b of depth direction of impurity concentration of epitaxial layer of actual SITimage sensor , way itshows in Figure 8 , receiving influence of ther mal processing in process ,in order from n'substrate Sb f acing toward epitaxial layer surface scattering todo, differ s from impurity concentration profile a at time of epitaxi al layer formation largely, haschanged gradually.

このようなエピタキシャル層不純物濃度のプロファイルと動作中のデバイス各部の電圧を考慮して、隣接 p'ゲート間に寄生チャネルが形成されるのを防ぐのに十分なトレンチ深さを決める必要がある。しかし、トレンチ下の Si 表面を反転させるための閾値電圧は、トレンチ下の SiO2/Si 界面準位密度等に依存して不安定であることも考えられ、したがって寄生チャネルの形成を完全に防ぐためには、十分余裕をもって深いトレンチを掘ることで対処せざるを得ない。

Considering voltage of device section which is a profile of the epitaxial layer impurity concentration a this way a nd in midst of operating, although it preventsfact that pa rasitism channel is formed between adjacent p'gate it is necessary todecide sufficient trench depth . But, threshold voltage in order inverting to do Sisurface under trench , depending on SiO2/Siinterface level density etc under tre nch , can think also that it isa unstable and therefore in order to prevent formation of parasitism channel comple tely, must cope by fact that deep trench is dug fully wit h Yutaka excessively.

ところが深いトレンチを形成するには異方性エッチングのための厚いマスクが必要であり、更に異方性エッチング処理にも長時間を要するため、プロセスの負担が増すのみならず、異方性エッチングによる損傷がデバイス特性に悪影響を与えることも考えられる。

Deep trench however is formed, for anisotropic etching t hick mask beingnecessary, in order furthermore to require lengthy even in anisotropic etching treatment, burden of process increases, furthermore, it is thoughtthat injury gi ves adverse effect to device characteristic with anisotropi c etching .

以上のように、SIT イメージセンサのセル間分離を行うためトレンチ分離方式を用いた場合、隣接するセルの p'ゲート間に電位差が生ずると、両 p'ゲートをソース・ドレインとし、トレンチ分離部を浮遊ゲートとする寄生 MOS トランジスタが ON することにより、隣接するセルの p'ゲート間が導通し、セル分離が阻害されるおそれがある。この寄生 MOS トランジスタが ON する閾値はトレンチ深さ(トレンチ底部での不純物濃度)、トレンチ下の SiO2/Si 界面での界面準位密度等に依存し、トレンチ深さを深くすれば閾値を高くすることができるが、トレンチ深さを深く形成する場合には、前記の如く種々の問題点が生ずる。本発明は、従来の SIT イメ-ジセンサの素子分離にトレンチ分離方式を用いた場合における上記問題点を解決するためになされたもので、SIT を光電変換素子として構成されるラインセンサあるいは固体撮像装置等のイメージセンサにおいて、デバイスの動作中のどのようなバイアス条

Like above, in order of SITimage sensor to separate bet ween cell , when trench isolation system is used, when voltage difference occurs between p'gate of the cell whic h is adjacent, both p'gate are designated as source *drain ,between of p'gate of cell which is adjacent parasitism MOS transistor whichdesignates trench isolation section a s floating gate by ON doing,does continuity , cell portio n separation is a possibility inhibition of being done. this parasitism MOS transistor as for threshold value which ON is done trench depth (impurity concentration with tre nch base),depends on interface level density etc with Si O2/Siinterface under trench , if trench depth is made dee p, but threshold value can be made high, when trench d epth is formeddeeply, as though it is a description abov e, various problem occurs. As for this invention, when tr ench isolation system is used for element separation of c onventional SITimage sensor ,being something which can be made above-mentioned Means to Solve the Problems which canbe put, in under which kind of bias condition

件下においても、トレンチ底部の Si 表面が反転して寄生チャネルが形成されることのないトレンチ分離による素子分離法を提供することを目的とする。

which is in midst ofoperating of device in line sensor o r solid image pickup apparatus or other image sensor wh ich configuration isdone, with SIT as photoelectric conve rsion element , Sisurface of trench base doing, inverting it designates that element separation method is offered w ith trench isolation which does not have fact that parasiti sm channel is formed as objective .

(問題点を解決するための手段及び作用)

means of Means to Solve the Problems And action)

上記問題点を解決するため、本願第 1 発明は、静電誘導トランジスタを光電変換素子として構成されるイメージセンサの第 1 不純物を含む第 1 半導体基板に溝を掘り、該溝の内面に絶縁膜を被着しポリシリコンで溝を埋め戻して素子を分離する方法において、前記溝に接する第 1 半導体基板の第 1 不純物濃度を高めて素子を分離するものであり、また第 2 発明は、静電誘導トランジスタを光電変換素子として構成されるイメージセンサにおいて、第 1 不純物を含む第 1 半導体基板に溝を掘り、該溝の側面にのみ絶縁膜を被着し、ポリシリコンで溝を埋め戻して素子を分離するものである。素子分離法を上記第 1 発明のように構成することにより、寄生 MOS トランジスタの閾値を上げることができるので、イメージセンサの動作中のどのようなバイアス条件下においても、隣接素子のゲート間のチャネルを常時オフにしておくことができ、良好な素子分離を行うことができる。また上記第 2 発明のように構成することにより、寄生 MOS トランジスタを除去して隣接素子のゲート間に寄生チャネルの形成を阻止することができ、良好な素子分離を計ることができる。

Above-mentioned Means to Solve the Problems , this ap plication first invention digging slot in first semiconducto r substrate whichincludes first impurity of image sensor which configuration is done with electrostatic induction tr ansistor as photoelectric conversion element , applying in sulating film to interior surface of the said slot and bury ing slot with polysilicon and resetting and regardingto m ethod which separates element , raising first impurity con centration of first semiconductor substrate which touches to aforementioned slot , being something whichseparates element , in addition as for second invention , It is som ething where you dig slot in first semiconductor substrate which includes first impurity , in image sensor which c onfiguration is done with electrostatic induction transistor as photoelectric conversion element , apply insulating fil m to only side face of the said slot , bury slot with pol ysilicon and reset and separates the element . element se paration method like above-mentioned first invention beca use it is possible, toincrease threshold value of parasitism MOS transistor , by configuration doing, in underwhiche ver kind of bias condition which is in midst of operating of the image sensor , it is possible, to designate channe l between gate of the adjacent element as regular off , it is possible to do satisfactory element separation . In ad dition like above-mentioned second invention removing p arasitism MOS transistor by the configuration doing, it is possible, can measure satisfactory element separation too bstruct formation of parasitism channel between gate of a djacent element .

(実施例)

以下実施例について説明する。

(Working Example)

You explain concerning below Working Example .

先に第 7 図(A),(B)において示した、隣接セルの p'ゲート G1,G2 とトレンチ分離部 15 で構成される寄生 MOS トランジスタのチャネル 18 を常時オフにしておくには、SIT アレイ動作中にトレンチ内ポリシリコン 19 に容量 C1,C2 を介して加わる負電圧よりも、寄生 MOS トランジスタの閾値を負側に設定しておけばよい。そしてこの寄生 MOS トランジスタは P チャネルなので、寄生 MOS トラ

First it showed Figure 7 (A), in (B), in p'gate G1, G2 and trench isolation section 15 of adjacent cell to desig nate channel 18 of parasitism MOS transistor which the configuration is done as regular off , during SITarray op erating through the capacity C1, C2 to polysilicon 19 ins ide trench , in comparison with negative voltage which j oins, threshold value of parasitism MOS transistor to neg ative side should have been set. Because and this parasit

ンジスタの閾値を上げるには、トレンチ直下のN型不純物濃度を上げればよいことになる。第1図は、トレンチ側面及び底部のSi表面付近のN型不鈍物濃度を上げた本願第1発明の実施例を示す図であり、第2図は、トレンチ底部のSi表面濃度を上げた、他の実施例を示す図である.第1図に示した構成のトレンチ分離構造を作成するには、まず酸化膜等をマスクにして、エピタキシャル層2を形成したS1基板にトレンチを掘り込み、トレンチ以外のSi表面をマスクしたまま、POCl3・リンドープSiO2,ヒ素ドープSiO2等を用いてトレンチ内側のSiにN型不純物をドープする。第1図において、25はこのドーピングによってN型濃度を上げた部分である。ドーピングの際に形成されたPSG,AsSGを除去し、薄い熱酸化膜26でトレンチ内Siを絶縁した後、ノンドープポリシリコン27でトレンチを埋め込む。その後、トレンチ内ポリシリコン27及びSi基板表面を酸化して厚い酸化膜28を形成し、次いで以後のプロセスに進み、p'ゲート29を形成する.

ism MOS transistor is Pchannel , to increase threshold value of the parasitism MOS transistor , n-type impurity concentration of trench directly below should have been increased especiallymeans. trench isolation structure of configuration which is shown in the.Figure 1 which is a figurewhich as for Figure 1 , n-type of Sisurface vicinity of trench side face and the base in figure which shows Working Example of this application first invention which increasednon- sluggishly thing concentration , as for Figure 2 , increased Sisurface concentration of trench base , shows other Working Example is drawn up, first with oxide film etc as mask , You dig trench in Sone reactor sheet which formed epitaxial layer 2 and are packed,doped you do n-type impurity in Si of trench inside making use of wayand POCl3* [rindoopu] SiO2, arsenic doped SiO2 etc which Sisurface other than trench the mask are done. In Figure 1 , 25 is portion which increased n-type concentration with the this doping . PSG , AsSG which was formed to case of doping is removed, withthin thermal oxide film 26 insulating after doing Si inside trench , the trench is imbedded with non doped polysilicon 27. After that, oxidation doing polysilicon 27 and Sisubstrate surface inside trench ,it forms thick oxide film 28, advances to process from now on next,forms p'gate 29.

一方、第2図に示したトレンチ分離構造を作成するには、厚い酸化膜等をマスクにしてSi基板にトレンチを掘り込み、トレンチ内Siを薄い熱酸化膜等31で絶縁した後、リンやヒ素の垂直イオン注入でトレンチ底部のSiにのみ選択的にN型不純物を導入する。この時導入したN型不純物によってトレンチ底部にN型層32が形成される。トレンチはノンドープポリシリコン33によって埋め戻され、トレンチ内ポリシリコン33とSi表面とを厚い酸化膜34で覆い、以後のプロセスに進み、p'ゲート35等を形成する。この構成例ではトレンチ底部にのみ選択的にN型層32が形成されるので、このN型層32とp'ゲート35とは直接には接触しない。したがって寄生MOSトランジスタの閾値を大きくとるためにN型層32の濃度を十分高く選んでも、p'ゲート35との耐圧は高くできる。なお、第1図に示した実施例では、N型層25とp'ゲート29とが直接接触しているため、N型層25の濃度を高くするのには限界がある。

On one hand, you dig trench in Sisubstrate with thick oxide film etcwhere trench isolation structure which is shown in Figure 2 is drawn up, as mask and are packed, Si inside trench you introduce selectively n-type impurity into only Si of trench base with 31 insulating after doing, withvertical ion implantation of phosphorus and arsenic such as thin thermal oxide film . n-type layer 32 is formed to trench base with n-type impurity which at timeof this is introduced. It buries trench with non doped polysilicon 33 and is reset, covers polysilicon 33 and Sisurface inside trench with thick oxide film 34, advances to process from now on, forms p'gate 35 etc. Because with this configuration example selectively n-type layer 32 is formed to only trench base ,this n-type layer 32 and p'gate 35 it does not contact direct. Therefore fully choosing concentration of n-type layer 32 highly inorder to take threshold value of parasitism MOS transistor largely, it can make pressure resistance of p'gate 35 high. Furthermore, with Working Example which is shown in Figure 1 , because n-type layer 25 and p'gate 29 direct contact it has done, in order to make the concentration of n-type layer 25 high, there is a limit .

先に述べたように、隣接セルのp'ゲート間に寄生MOSトランジスタが形成されることによって、両p'ゲート間にチャネルができるものであるから、このチャネルの発生を阻止するには寄生MOSトランジスタを除去してやればよい。第3図

As expressed before, by fact that parasitism MOS transistor is formed between the p'gate of adjacent cell , because it is something which can designate the channel as between both p' [gee] *, occurrence of this channel isobstructed, removing parasitism MOS transistor . Figure 3 (A

(A)は、このように構成した本願第2発明の実施例を示す図である。トレンチ側面41は薄い熱酸化膜等の絶縁膜42で絶縁し、トレンチ底部43は基板のSiが露出した状態でトレンチ内にノンドープポリシリコン44を埋め込む。このトレンチ分離構造の等価回路を第3図(B)に示す。両p'ゲートG1,G2が容量C1,C2を介してノンドープポリシリコン44に接続される。ノンドープポリシリコン44は極めて大きな抵抗Rをもつ導体とみなされるので、この抵抗Rを通してドレイン電圧V0に接続される。

), this way is figure which shows Working Example of the this application second invention which configuration is done. insulating it does trench side face 41 with thin thermal oxide film or other insulating film 42, trench base 43 with the state which Si of substrate exposes imbeds non doped polysilicon 44 inside the trench . equivalent circuit of this trench isolation structure is shown in Figure 3 (B). Both p' [gee] * G1, G2 through capacity C1, C2, it is connected to the non doped polysilicon 44. Because non doped polysilicon 44 is regarded conductor which quite has large resistor R, it is connected to drain voltage V0 through this resistor R.

この実施例では、トレンチ底部43は、隣接セルのp'ゲート間に極めて大きな電位差が存在し、p'ゲート45とn'エピタキシャル層2の間の空乏層がトレンチ底部に達することがない限りN型のままであり、したがって、チャネルは生じない。この時、トレンチ底部43のSi電位はVpである。第3図(B)において46で示した部分がトレンチ底部43のSiに相当する。

With this Working Example , as for trench base 43, quite large voltage difference exists between p'gate of adjacent cell , if there are not times when depletionlayer between p'gate 45 and n'epitaxial layer 2 reaches to trench base itcontinues to be a n-type , therefore, channel does not occur. At time of this , Sivoltage of trench base 43 is Vp. portion which is shown with 46 in Figure 3 (B) is suitable to the Si of trench base 43.

ところで、この構成においてトレンチが浅かったり、エピタキシャル層2の不純物濃度が低く容易に空乏化する場合には、p'ゲート45とエピタキシャル層2の間にできる空乏層がトレンチ底部43にまで達することがありうる。この時、Si基板2とポリシリコン44の界面付近に存在する準位で発生する過剰な電荷により、大きな暗出力を発生するおそれがあると同時に、この空乏層が隣のセル内に侵入するとスミアの原因になり、極端な場合には隣接セルのp'ゲート間にバルクチャネルを形成する可能性も出てくる。

When by way, trench to be shallow in this configuration , impurity concentration of epitaxial layer 2 to be low easily depletion it does, can be p'gate 45 and thedepletion layer which can be made between epitaxial layer 2 reaching to the trench base 43. When there is a possibility of generating large darkness output attime of this , due to excessive charge which occurs with level which exists in interface vicinity of Sisubstrate 2 and polysilicon 44, whensimultaneously, this depletion layer invades inside cell ofnext door, it becomes cause of smearing , in extreme case also the possibility which forms bulk channel between p'gate of adjacent cell comes out.

第4図に示す実施例が、この欠点を解決したものである。この実施例は厚い酸化膜をマスクにしてSi基板にトレンチを掘り込み、トレンチ表面を酸化した後、トレンチ底部の酸化膜のみ異方性エッチングで除去し、トレンチ底部にN型不純物をイオン注入してから、ノンドープポリシリコン51で埋め込むものである。この構造ではトレンチ側面は絶縁膜52で保護され、隣接セルのp'ゲート53,54が接触することはないし、トレンチ底部56にはN型層55が形成され、p'ゲート53あるいは54とn-エピタキシャル層2の間にできる空乏層が、トレンチ底部56を空乏化することはない。またこの時のN型層の濃度は十分高く選ぶことができるので、確実に素子分離ができると同時に、p'ゲート53,54とN型層55とが直接接触することがないので、両者の接合耐圧は十分高くとることができる.

Working Example which is shown in Figure 4 , is something which solves the this deficiency . this Working Example to dig trench in Sisubstrate with thick oxide film as the mask , to be packed, oxidation after doing trench surface , only oxide film of trench base to remove with anisotropic etching , after ion implantation doing n-type impurity in trench base , it is something which it imbeds with non doped polysilicon 51. With this structure as for trench side face it is protected with insulating film 52, thereare not times when p'gate 53, 54 of adjacent cell contacts depletion layerwhere and, n-type layer 55 is formed by trench base 56, p'gate 53 or canmake between 54 and n- epitaxial layer 2, are not times when depletion it does trench base 56. In addition because concentration of n-type layer at time of this can choose fully highly, when element separation is possible securely,because simultaneously, p'gate 53, 54 and n-type layer 55 are not timeswhen direct contact it does, connecting pressure resistance of both can take the fully highly.

更に、プロセス中の熱工程を通して N 型層 55 からノンドープポリシリコン 51 へ N 型不純物が拡散することにより、ポリシリコン 51 がドーピングされ、ポリシリコン全体が n'基板 1 と同じ正電位にバイアスされる。

Furthermore, polysilicon 51 doping is done from n-type l ayer 55 n-type impurity by scattering doing to non dope d polysilicon 51 through heat step in process , the polys ilicon entirety bias is done in same positive voltage as n' substrate 1.

このバイアスによりトレンチ側面の Si57 は、p'ゲート 53,54 の電位にあまり影響されずに蓄積層にしておくことができる。これはトレンチ側面の Si O2 絶縁膜 52 と Si57 の界面に存在する界面準位を常に電子で埋めておくことができるので、界面準位からの過剰な電荷発生を防ぐことができ、したがって暗出力を小さく抑えるのに有効である。第 4 図に示した第 2 実施例の効果、すなわち、トレンチ底部を常に N 型に保つことによって確実に素子分離ができ、またトレンチ内ポリシリコンが n'基板と同じ正電位になるのでトレンチ側面の Si を蓄積層とすることができ、更に p'ゲートとトレンチ底部の n'拡散層との耐圧を高くすることができるという効果を、より確実に引き出すことができるようにした他の実施例を第 5 図に示す。

As for Si57 of trench side face , excessively without bei ng influenced ispossible fact that it makes compilation la yer to voltage of p'gate 53, 54 with this bias . Because as for this it is possible, to bury SiO2insulating film 52 of trench side face and interface level which exists in in terface of Si57 with normally electron it ispossible to pr event excessive charge occurrence from interface level , t hereforealthough darkness output is held down small, it i s effective. Effect of second Working Example which is shown in Figure 4 , element separation to bepossible sec urely by fact that namely, trench base is maintained at t he normally n-type , in addition because polysilicon insid e trench becomes same positive voltage as n'substrate , it is possible, furthermore can make pressure resistance of p'gate and n'diffusion layer of trench base high to desig nate Si of trench side face as compilation layer, effect t hat, Other Working Example which it can pull out more securely, requires is shownin Figure 5 .

この実施例は第 5 図に示すように、ドープトポリシリコン 61 からの拡散によりトレンチ底部に n' 拡散層 62 を形成するものであり、トレンチの埋め込みにドープトポリシリコンを使う以外は、第 3 図に示した第 1 実施例と同様の方法で製作される。ドープトポリシリコン 61 は、CVD 時にリン等の N 型不純物を含む膜として堆積されてもよいし、最初にノンドープポリシリコンとして堆積してから、Pocl3 等で N 型にドープしてもよい。このようにドープトポリシリコン 61 でトレンチを埋め戻すことにより、ポリシリコンを低抵抗導体とみなすことができると同時に、高濃度 N 型不純物拡散源として扱うことができる。なお 63 は p'ゲート, である。

As for this Working Example as shown in Figure 5 , be ing something which forms n'diffusion layer 62 in trench base with scattering from doped polysilicon layer 61, ot her than using doped polysilicon layer in pad of trench , it is produced with method whichis similar to first Wor king Example which it shows in Figure 3 . After may b e accumulated and first as membrane which includes the phosphorus or other n-type impurity at time of CVD ac cumulating doped polysilicon layer 61, as non doped pol ysilicon doped it is possible to do to n-type with such a s Pocl3. this way when it buries trench it can regard pol ysilicon the low resistance conductor with doped polysilic on layer 61 and by resetting, simultaneously, it is possibl eto handle as high concentration n-type impurity diffusio n source . Furthermore 63 is p'gate , .

また第 4 図に示した第 2 実施例のイオン注入によってトレンチ底部に n'層を形成する方法では、トレンチ形状やイオンの入射角度等によってトレンチ側面にも N 型不純物が導入されるおそれがあるので、p'ゲート 53,54 と N 型層 55、すなわちドレイン基板 1 との耐圧低下を招く危険性がある。しかし、この第 5 図に示した第 3 の実施例では、このような不都合は生じない.

In addition because with method which with ion implant ation of second Working Example which is shown in Fi gure 4 forms n' layer in trench base , n-type impurity b eing introduced into also trench side face with such as tr ench shape and incident angle of ion there is a possibilit y, p'gate 53, 54 and n-type layer 55, namelythere is a ri sk which causes pressure resistance decrease of drain sub strate 1. But, with Working Example of third which is s hown in this Figure 5 , as for undesirable a this way it does not occur.

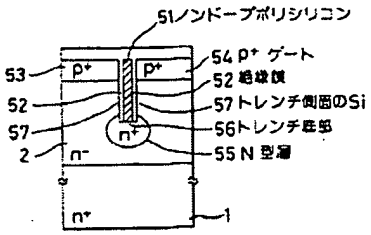
(発明の効果)

(Effect of Invention)

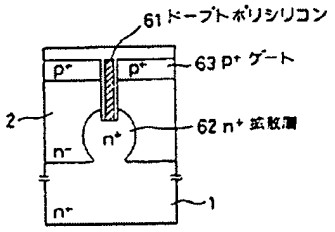
以上実施例に基づいて説明したように、本願各発明によれば、高密度 SIT イメージセンサの素

As explained on basis of or more Working Example , according to this application each invention, in slot separati high dens n of 1;mu ate of base here not t type under sensor op ism chann ient isgon

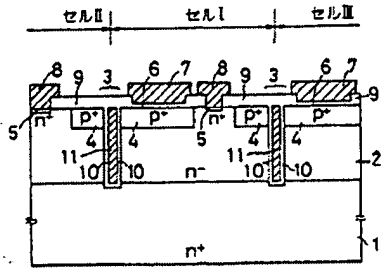
第 4 図



第 5 図

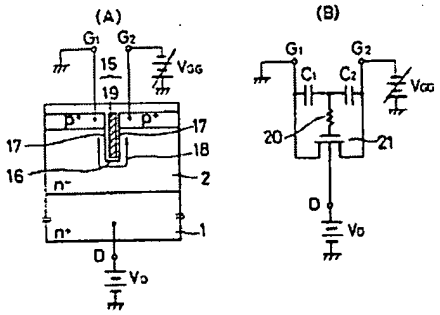


第 6 図

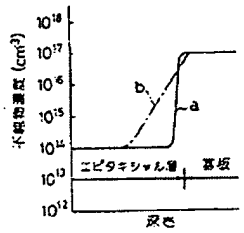


which sho th one Wo n , as for tline cross ng Exampl ure 3 (B) mage senso n second i how equiva show the second W figure and SITimage s invention , ure 7 (A) nventional iagram , F asitism cha gure 6 , a it circuit , th direction SITimage

第 7 図



第 8 図



r n'epitaxia nal oxide f ilm , 29 a 2 n-type l xide film , , 42 as fo nondoobup or non do 3, 54 as fo nch base , n'diffusion

特許出願人 オリンパス光学工業株式会社代理人弁理士最上健治

patent applicant Olympus Optical Company, Ltd. (DB 69-053-6248) type company representative patent agent top most Kenji